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(54) **High-frequency power divider and combiner**

Schaltung zum Aufteilen oder Zusammenführen von Hochfrequenzleistung

Circuit de combinaison de distribution de puissance à haute fréquence

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US-A- 4 893 093
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US-A- 5 032 798

- **IEEE 1990 INTERNATIONAL RADAR CONFERENCE May 7-10,1990,Arlington,US;IEEE,New York,US,,1990 J.D. HAY et al.:"The exploratory development of a high power S-band solid state radar transmitter" pages 135-140**

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Description

The present invention relates to a high-frequency power divider and combiner, and more specifically to a circuit for dividing and combining high-frequency power when a plurality of power amplifiers are parallel-operated, e.g. as known from US-A-5 032 798.

As power dividing and combining circuits for parallel-operating power amplifiers and combining together outputs produced from the power amplifiers so as to obtain large power, there have heretofore been used a 3 dB coupler type power divider and combiner, a Wilkinson's power divider and combiner, and an impedance transformer type power divider and combiner.

In a power amplifying apparatus of a type wherein a plurality of power amplifiers are parallel-operated to generate output power, which is then combined so as to produce large power, allowable out power is often controlled by changing the number of the power amplifiers. A description will now be made, as an illustrative example, of a case in which input and output impedance in circuits are set to 50 Ω, two, three or four power amplifiers are parallel-operated to thereby control allowable output power of a power amplifying apparatus.

With the 3 dB coupler type power divider and combiner is used, the power can be efficiently divided and combined only when the number of power amplifiers to be parallel-operated is 2^n. On the other hand, with the Wilkinson's power divider and combiner is used, the power can be efficiently divided and combined when the number of parallel operating power amplifiers is an even number. In either case where the number of power amplifiers to be parallel-operated is four, the power amplifiers can be efficiently parallel-operated by using a 4-way divider and a 4-way combiner. However, when the number of the power amplifiers is reduced from four to three or two, the power is used up by resistances as dummy loads for absorbing unbalanced power, which are used to obtain isolation between terminals of dividers and between those of combiners. Therefore, a power loss of about 2.5 dB is developed when the three power amplifiers are used, whereas a power loss of about 6.0 dB is developed when the two power amplifiers are used.

In order to efficiently divide the power and combine it in 2-way combination form, it is necessary to replace the divider and the combiner with a 2-way divider and a 2-way combiner respectively. When the divider and the combiner are replaced by others respectively, the operation of a power amplifying apparatus should be temporarily stopped. Therefore, the 3 dB coupler type power divider and combiner and the Wilkinson's power divider and combiner are not suited to a method of making the change in the number of the units of the power amplifiers to thereby adjust or control the allowable output power of the apparatus.

Accordingly, impedance transformer type 4-way divider and 4-way combiner will be shown in FIG. 6(A) as one example. In FIG. 6(A), D indicates a power dividing circuit (hereinafter called merely a "divider") and S indicates a power combining circuit (hereinafter called merely a "combiner"). In addition, A_1 through A_4 indicate power amplifiers respectively. However, the impedance transformer type divider and combiner, different from the 3 dB coupler type power divider and combiner and the Wilkinson's power divider and combiner, provide no resistance as a dummy load for unbalanced power absorption, but only an impedance matching function is provided and hence no isolation is obtained between terminals. Therefore, the isolation between adjacent output terminals for outputs 1 through 4 of the divider and the isolation between adjacent input terminals for inputs 1 through 4 of the combiner are obtained from either isolators or circulators I provided at inputs and outputs of respective power amplifiers Ai as shown in FIG. 6(B).

The combiner S and the divider D are identical in principle to each other. A description will therefore be made of the combiner S as an illustrative example. Transmission lines Ws_1 through Ws_4 each having an impedance of 50 Ω and a line length of $n\lambda/2$ (where n = positive integer and λ = wavelength of a used frequency) are provided between the respective input terminals of the combiner S and a combining point P thereof. Since the lines of 50 Ω impedance are 4-way combined, the impedance at the combining point P is brought to 12.5 Ω (= 50 Ω/4).

An impedance transformer is used to convert or transform the impedance at the combining point P into output impedance of 50 Ω. For example, the impedance transformer is composed of a transmission line Ws_5 having the impedance of 25 Ω and a line length of λ/4. Incidentally, the divider D is also constructed in a manner similar to the combiner S. In this case, transmission lines Wd_1 through Wd_4 correspond to the transmission lines Ws_1 through Ws_4 and a transmission line Wd_5 serving as the impedance transformer corresponds to the transmission line Ws_5. By setting the combiner S and the divider D in this way, a division loss is 0 db whereas a combination loss is 0 dB, which result in the total loss of 0 dB.

A description will now be made of a case in which the control of allowable output power is carried out by making a change in the number of power amplifiers. As shown in FIG. 7, one of input terminals of a 4-way combiner S is opened and three power amplifiers are connected in parallel to the corresponding input terminals so as to produce the output of the 4-way combiner in the form of 3-combination. The length of each of transmission lines, which extend from the power amplifiers A_1, A_2, A_3 to a combining point P, is $n\lambda/2$. Thus, the impedance as seen in the direction of the opened input terminal of the 4-way combiner from the combining point P is equivalently brought to infinity. Therefore, the impedance at the combining point P reaches about 16.7 Ω (= 50 Ω/3).

Further, an impedance transformer, which extends from the combining point P to the output terminal, is constructed

so as to transform 12.5 Ω into 50 Ω. Thus, when this impedance transformer is used so as to transform 16.7 Ω into 50 Ω, the reflection coefficient produced due to impedance mismatching is determined by th following equation:

$$\text{Reflection coefficient} = (Z_L - Z_0)/(Z_L + Z_0)$$

$$= (16.7-12.5)/(16.7+12.5)$$

$$= 0.144$$

The reflection loss produced due to the impedance mismatching is determined by the following equation:

$$\text{Reflection loss} = 10 \log[1/(1-\text{reflection coefficient}^2)]$$

$$= 10 \log[1/(1-0.144^2)]$$

$$= 0.09 \text{ dB}$$

Thus, the reflection loss is brought to about 0.09 dB.

The divider D also gives rise to the reflection loss in a manner similar to the combiner S. Therefore, the reflection loss is doubled over the entire device, that is, the reflection loss amounts to about 0.18 dB.

When the combiner S is used as a 2-combiner in the same manner as described above, the impedance at a combining point P is brought to 25 Ω (= 50 Ω/2) as shown in FIG. 8. Therefore, the loss produced due to impedance mismatching of an impedance transformer is brought to about 0.5 dB. Thus, the loss in the combiner S and the divider D reaches about 1.0 dB in total.

Even when the 4-way combiner is used as a 3-way combiner or a 2-way combiner as described above, the power combination can be made although only the mismatch loss due to the impedance transformer is produced. The input power division can also be carried out in a manner similar to the power combination. However, a division loss and a combination loss due to mismatching increase when the number of divisions and the number of combinations are reduced.

It is a general aim of the present invention to provide a high-frequency power divider and combiner capable of dividing and combining power at a reduced loss for use in a power amplifying apparatus in which a plurality of power amplifiers are parallel-operated and the output power thereof is controlled by changing the number of the power amplifiers.

In one aspect therefore the present invention provides, in a power amplifying apparatus which includes high-frequency power amplifiers parallel-operated in a range between M and N (M and N: positive integers and M<N) both indicative of the number of the power amplifiers and which makes a change in the number of the parallel-operated power amplifiers to thereby control output power, a high-frequency power divider and combiner comprising a power dividing circuit having an impedance transformer set in such a manner that the power loss is minimized by assigning the intermediate number K (positive integer) between M and N both of which indicate the number of divisions and having N output terminals, and a power combining circuit having an impedance transformer set in such a manner that the power loss is minimized by assigning the intermediate number K corresponding to the number of combinations and having N input terminals.

The present invention can also provide a high-frequency power divider and combiner wherein a plurality of transmission lines serving as an impedance transformer each having a predetermined impedance and a predetermined line length are connected from respective input terminals of the combiner, the impedance transformation of the impedance transformer is separately made between respective transmission lines electrically connected to the corresponding transmission lines and a combining point and an impedance transformer is electrically connected to the combining point so as to carry out the impedance transformation.

The above and other objects, features and advantages of the present invention will become apparent from the following description and the appended claims, taken in conjunction with the accompanying drawings in which a preferred embodiment of the present invention is shown by way of illustrative example.

FIG. 1 is a block diagram showing the structure of one embodiment of the present invention;

FIG. 2 is a block diagram illustrating the structure of the embodiment shown in FIG. 1, which is applied to a 4-way division and a 4-way combination;

FIG. 3 is a block diagram depicting the structure of the embodiment shown in FIG. 1, which is applied to a 2-way division and a 2-way combination;

FIG. 4 is a diagram showing the structure of a combiner wherein the impedance transformation of an impedance transformer employed in the embodiment shown in FIG. 1 is performed between respective input terminals and a combining point and between the combining point and an output terminal;

FIG. 5 is a diagram illustrating the structure of another combiner wherein the impedance transformation of the impedance transformer employed in the embodiment shown in FIG. 1 is carried out between respectiv input terminals and a combining point;

FIG. 6(A) is a block diagram depicting the structure of a conventional example illustrative of impedance transformer type 4-way divider and 4-way combiner;

FIG. 6(B) is a block diagram showing the structure of a conventional example in which isolation between re spective output terminals of a divider and isolation between respective input terminals of a combiner are obtained by isolators I or circulators electrically connected to inputs and outputs of respective power amplifiers Ai;

FIG. 7 is a block diagram showing the structure of the conventional example depicted in FIG. 6(A), which is applied to a 3-way division and a 3-way combination; and

FIG. 8 is a block diagram illustrating the structure of the conventional example shown in FIG. 6(A), which is applied to a 2-way division and a 2-way combination.

FIG. 1 is a block diagram showing the structure of one embodiment of the present invention.

The present embodiment illustrates cases in which the number of power combinations ranges from 2 to 4.

In the present embodiment, as shown in FIG. 1, impedance transformer type 4-way divider and 4-way combiner are constructed in such a manner that one of input terminals and one of output terminals are opened, power amplifiers A_1, A_2 and A_3 are parallel-connected to each other and the total power loss is minimized when the output is represented in the form of a 3-way combination.

The 4-way combiner S_1 and the 4-way divider D_1 are identical in principle to each other. A description will therefore be made of the 4-way combiner S_1 as an illustrative example.

Let's now assume that the impedance and length of each of transmission lines Ws_1 to Ws_4, which extend from the power amplifiers A_1 to A_4 to a combining point P, are 50 Ω and $n\lambda/2$ respectively in a manner similar to FIG. 6(A). Outputs of impedance 50 Ω are 3-way combined and result in the impedance of about 16.7 Ω at the com bining point P. An impedance transformer, which converts, i.e., transforms the impedance of 16.7 Ω at the combining point P into the 50 Ω output impedance, is constructed of a transmission line Ws_{51} whose impedance and length are 28.9 Ω and $\lambda/4$ respectively.

When the 4-way combiner S_1 is made up of three parallel-connected power amplifiers and the output of the 4-way combiner S_1 is represented in the form of a 3-way combination, the impedance as seen in the direction of provision of the opened input terminal from the combining point P of the 4-way combiner S_1 is equivalently regarded as infinite. Further, the loss of the impedance transformer is zero. Since the output of the 4-way combiner S_1 is represented in the form of the 3-way combination as described above, no mismatching is developed and the combination loss is theoretically 0 dB.

Further, the 4-way divider D_1 is also identical in structure to the 4-way combiner S_1. Transmission lines Wd_1 to Wd_4 correspond to the transmission lines Ws_1 to Ws_4 and a transmission line Wd_{51} serving as an impedance transformer corresponds to the transmission line Ws_{51}. Thus, the division loss is 0 dB and the sum of the division loss and the combination loss is also 0 dB.

When the output of the above 4-way combiner S_1 is represented in the form of a 4-way combination as shown in FIG. 2, another power amplifier is added to the three power amplifiers shown in FIG. 1. In this case, the power loss at the combining point P, which is developed due to mismatching is brought to about 0.09 dB. Similarly to the 4-way combiner S_1, 4-way divider D_1 is also constructed in such a manner that the power loss is brought to about 0.09 dB. Accordingly, the power loss of the entire apparatus reaches about 0.18 dB.

When the output of the above 4-way combiner S_1 is represented in the form of a 2-way combination as shown in FIG. 3, one power amplifier is removed from the three power amplifiers shown in FIG. 1 and the impedance at the combining point P is brought to 25 Ω. In addition, the power loss due to the mismatching of the impedance transformer is brought to about 0.17 dB. Similarly to the combiner S_1, divider D_1 shown in FIG. 3 is also constructed in such a manner that the power loss is brought to about 0.17 dB. Thus, the power loss of the entire device reaches about 0.34 dB.

If the power loss is minimized as described above when the input of the 4-way divider D_1 is represented in the form of 3-way division and the output of the 4-way combiner S_1 is represented in the form of a 3-way combination, then the power combination can be made at a low loss when the number of the power amplifiers to be parallel-operated is 4, 3 and 2. It is apparent that the power combination can be performed at the low loss if the loss at the power combination is compared with the cases developed in the conventional examples shown in FIGS. 6(A), 6(B), 7 and 8.

When the divider and combiner according to the present embodiment are now applied to a method of starting the operations of two power amplifiers upon installation and increasing the number of the power amplifiers in order of 3, 4, at a certain period after the installation of the two power amplifiers so as to make an increase in the output power, it is unnecessary to make changes in the divider D_1 and the combiner S_1 when the number of the power amplifiers has been increased. Therefore, the number of the power amplifiers can be increased without temporarily inactivating the power amplifiers.

Therefore, the divider and combiner according to the present embodiment are most suitable for use with, e.g., a base station used to provide mobile telephone service, of a type wherein the station is first operated by a small number of power amplifiers upon installation and the number of the power amplifiers is then increased successively so as to increase power to be transmitted to mobile stations. If the divider and combiner are employed in a system of a type wherein the transmission of a radio wave cannot b stopped even a moment as in the base station, then an increase in the power to be transmitted can be made by simply increasing the number of the power amplifiers without stopping the transmission even a moment.

The above-described embodiment has shown, as an illustrative example, a case in which the two to four power amplifiers are parallel-operated. However, the number of the power amplifiers to be parallel-operated is not necessarily limited to these numbers and hence any number of power amplifiers can be used. When the number of power amplifiers to be parallel-operated ranges from M to N, the impedance transformer may be constructed by selecting the optimum value in such a manner that the power loss is minimized by an intermediate number K (positive integer) between M and N.

Incidentally, the above-described embodiment has shown the combiner in which the impedance transformation by the impedance transformer is carried out between the combining point P and the output terminal. Further, the present embodiment has also shown the divider in which the impedance transformation is made between the input terminal and the dividing point.

As shown in FIG. 4, however, the impedance transformation can also be made between respective input terminals and a combining point P and between the combining point P and the output terminal. In the illustrated example, transmission lines Ws_{11}, Ws_{12}, Ws_{13}, Ws_{14} each of which has the impedance of 50 Ω and a line length of $\lambda/4+n\lambda/2$, are connected from the respective input terminals of the combiners. Further, an impedance transformer is used to transform the impedance of 50 Ω into the impedance of 100 Ω for each transmission line. As an illustrative example, the impedance transformer is composed of transmission lines Ws_{21}, Ws_{22}, Ws_{23}, Ws_{24} each having an impedance of 70.7 Ω and a line length of $\lambda/4$, which are electrically connected to their corresponding transmission lines Ws_{11}, Ws_{12}, Ws_{13}, Ws_{14} so as to perform the impedance transformation.

Now, the impedance at the combining point P is brought to 25 Ω (= 100 Ω/4). An impedance transformer is used to transform the impedance of 25 Ω at the combining point P into that of 50 Ω. For example, this type of impedance transformer is constructed of a transmission line Ws_{52} which has the impedance of 35.4 Ω and a line length of $\lambda/4$. Thus, the impedance transformation can be made between the respective input terminals and the combining point P. The divider D_1 can also be treated in the same manner as the combiner.

As also shown in FIG. 5, the impedance transformation can also be carried out between respective input terminals and a combining point P. In the illustrated example, transmission lines Ws_{11}, Ws_{12}, Ws_{13}, Ws_{14} each of which has the impedance of 50 Ω and a line length of $\lambda/4+n\lambda/2$, are connected from respective input terminals of the 4-way combiner. Further, an impedance transformer is used to transform the impedance of 50 Ω into the impedance of 200 Ω for each transmission line. As one example, this type of impedance transformer is composed of transmission lines Ws_{31}, Ws_{32}, Ws_{33}, Ws_{34} each having the impedance of 100 Ω and a line length of $\lambda/4$, which are electrically connected to their corresponding transmission lines Ws_{11}, Ws_{12}, Ws_{13}, Ws_{14} so as to carry out the impedance transformation.

Now, the impedance at a combining point P is brought to 50 Ω (=200 Ω/4). Since the impedance at the combining point P is 50 Ω, a transmission line Ws_{53} having an impedance of 50 Ω and an optional line length electrically connects the combining point P with the output terminal. Thus, the impedance transformation can be carried out between the respective input terminals and the combining point P. The divider D_1 can also be treated in the same manner as the combiner.

According to the present invention, as has been described above, there are provided a power dividing circuit having an impedance transformer set in such a manner that the power loss is minimized by assigning an intermediate number K (positive integer) between M and N both of which indicate the number of divisions and having N output terminals, and a power combining circuit having an impedance transformer set in such a manner that the power loss is minimized by assigning the intermediate number K corresponding to the number of combinations and having N input terminals. In addition, the number of power amplifiers to be parallel-operated is changed to make a change in the output power. Therefore, with a small number of power amplifiers first started upon installation to which an increase or decrease in the number of power amplifiers to be parallel-operated is made when a certain period has elapsed after the initial installation, an increase in the power loss can be reduced.

It is also unnecessary to make changes in the divider and combiner each time the increase and decrease in the number of the power amplifiers to be parallel-operated is made. Therefore, if the divider and combiner are employed in the system wherein the transmission of the radio wave cannot be stopped even a moment as in the base station used to provide the vehicle radiotelephone service or communication, then an increase in the power to be transmitted can be made by simply increasing the number of the power amplifiers. Thus, such an increase in the transmission power can be carried out without stopping the power transmission even a moment.

Further, M power amplifiers are parallel-operated at all times provided that one of these is operated as a mounted

spare power amplifier. However, if M-1 power amplifiers are parallel-operated in such a manner that their characteristics are satisfied, then a failure in a single power amplifier can be processed without inactivating the device.

In the above, a description has been made of a case in which an input/output int rface in a circuit has the impedance of 50 Ω. It is however needless to say that an impedance value other than 50 Ω may be used.

Claims

1. A high-frequency power divider and combiner for use in a power amplifying apparatus which includes a plurality of power amplifiers (A_1, A_2, A_3, A_4) parallel-operated in a range between M and N - where M and N are positive integers and M<N - both indicative of the number of the power amplifiers and which makes a change in the number of the parallel-operated power amplifiers to thereby,control output power, said high-frequency power divider and combiner characterised by:

   a power dividing circuit (D_1) having an impedance transformer (Wd_{51}) set in such a manner that the power loss is minimized by assigning an intermediate number K being a positive integer between M and N both of which indicate the number of divisions and having N output terminals; and
   a power combining circuit (S_1) having an impedance transformer (Ws_{51}) set in such a manner that the power loss is minimized by assigning said intermediate number K corresponding to the number of combinations and having N input terminals.

2. A high-frequency power divider and combiner according to claim 1, wherein a plurality of transmission lines (Ws_{21}, Ws_{22}, Ws_{23}, Ws_{24}) serving as an impedance transformer each having a predetermined impedance and a predetermined line length are connected from respective input terminals of said combiner, the impedance transformation of said impedance transformer is separately made between respective transmission lines electrically connected to the corresponding transmission lines (Ws_{11}, Ws_{12}, Ws_{13}, Ws_{14}) and a combining point (P) and an impedance transformer (Ws_{52}; Ws_{53}) is connected to said combining point (P) so as to carry out the impedance transformation.

Patentansprüche

1. Hochfrequenz-Leistungsteiler und -summierer zur Verwendung in einer Leistungsverstärkervorrichtung, die mehrere Leistungsverstärker (A_1, A_2, A_3, A_4) enthält, die in einem Bereich zwischen M und N - mit M und N als natürlichen Zahlen und M < N - betrieben werden, die beide die Anzahl von Leistungsverstärkern angeben, und bei der eine Änderung der Anzahl der parallel betriebenen Leistungsverstärker zur Steuerung der Ausgangsleistung erfolgt, wobei der Hochfrequenz-Leistungsteiler und -summierer gekennzeichnet ist durch

   - eine Leistungsteilerschaltung (D_1) mit einem Impedanzwandler (Wd_{51}), welcher derart eingestellt ist, daß der Leistungsverlust dadurch minimiert wird, daß eine Zwischenzahl K als natürliche Zahl zwischen M und N zugewiesen wird, die beide die Anzahl von Teilungen bei N Ausgangsanschlüssen angeben; und

   - eine Leistungssummierschaltung (S_1) mit einem Impedanzwandler (Ws_{51}), welcher derart eingestellt ist, daß der Leistungsverlust dadurch minimiert wird, daß die Zwischenzahl (K) entsprechend der Anzahl von Kombinationen bei N Eingangsanschlüssen zugewiesen wird.

2. Hochfrequenz-Leistungsteiler und -summierer nach Anspruch 1, bei dem eine Mehrzahl von Übertragungsleitungen (Ws_{21}, Ws_{22}, Ws_{23}, Ws_{24}), die als Impedanzwandler mit jeweils einer vorbestimmten Impedanz und einer vorbestimmten Leitungslänge dienen, an den jeweiligen Eingangsanschluß des Summierers angeschlossen sind, wobei die Impedanzwandlung durch den Impedanzwandler getrennt erfolgt zwischen den jeweiligen Übertragungsleitungen, die elektrisch mit den zugehörigen Übertragungsleitungen (Ws_{11}, Ws_{12}, Ws_{13}, Ws_{14}) verbunden sind, und einem Summierpunkt (P), wobei ein Impedanzwandler (Ws_{52}; Ws_{53}) an den Summierpunkt (P) angeschlossen ist, um die Impedanzwandlung durchzuführen.

Revendications

1. Un diviseur et combinateur de puissance haute fréquence pour utilisation dans un appareil d'amplification de puissance qui comprend une pluralité d'amplificateurs de puissance (A_1, A_2, A_3, A_4) fonctionnant en parallèle dans

une gamme comprise entre M et N, où M et N sont des entiers positifs représentant le nombre d'amplificateurs de puissance et où M<N, et qui fait varier le nombre d'amplificateurs de puissance fonctionnant en parallèle afin de faire varier en correspondance la puissance de sortie, le diviseur et combinateur de puissanc à haute fréquence étant caractérisé par:

- un circuit de division de puissance (D_1) présentant un transformateur d'impédance (Wd_{51}) réglé d'une telle façon que la perte de puissance soit minimisée en choisissant un chiffre intermédiaire K, K étant un entier positif compris entre M et N, tous deux indicatifs du nombre de divisions et présentant N bornes de sortie; et
- un circuit de combinaison de puissance (S_1) présentant un transformateur d'impédance (Ws_{51}) réglé d'une telle façon que la perte de puissance soit minimisée par le choix dudit nombre intermédiaire K, correspondant au nombre de combinaisons, et présentant N bornes d'entrée.

2. Un diviseur et combinateur de puissance haute fréquence selon la revendication 1, dans lequel une pluralité de lignes de transmission (Ws_{21}, Ws_{22}, Ws_{23}, Ws_{24}) fonctionnant comme transformateur d'impédance et présentant chacune une impédance prédéterminée et une longueur de ligne prédéterminée sont raccordées en partant des bornes d'entrée respectives dudit combinateur, la transformation d'impédance dudit transformateur d'impédance étant réalisée séparément entre des lignes de transmission respectives reliées électriquement aux lignes de transmission correspondantes (Ws_{11}, Ws_{12}, Ws_{13}, Ws_{14}) et un point de combinaison (P), un transformateur d'impédance (Ws_{52}; Ws_{53}) étant raccordé audit point de combinaison (P) afin de réaliser la transformation d'impédance.

FIG.1

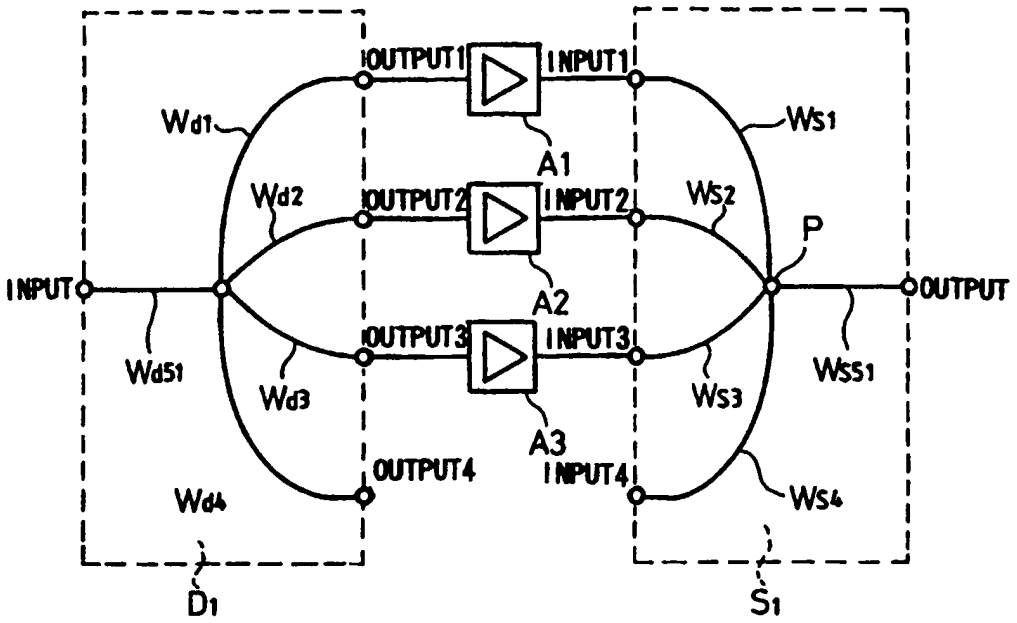

OUTPUT1
INPUT1
Wd1
Ws1
A1
Wd2
OUTPUT2
INPUT2
Ws2
P
INPUT
OUTPUT
A2
OUTPUT3
INPUT3
Wd51
Ws51
Wd3
Ws3
A3
OUTPUT4
INPUT4
Wd4
Ws4
D1
S1

FIG.2

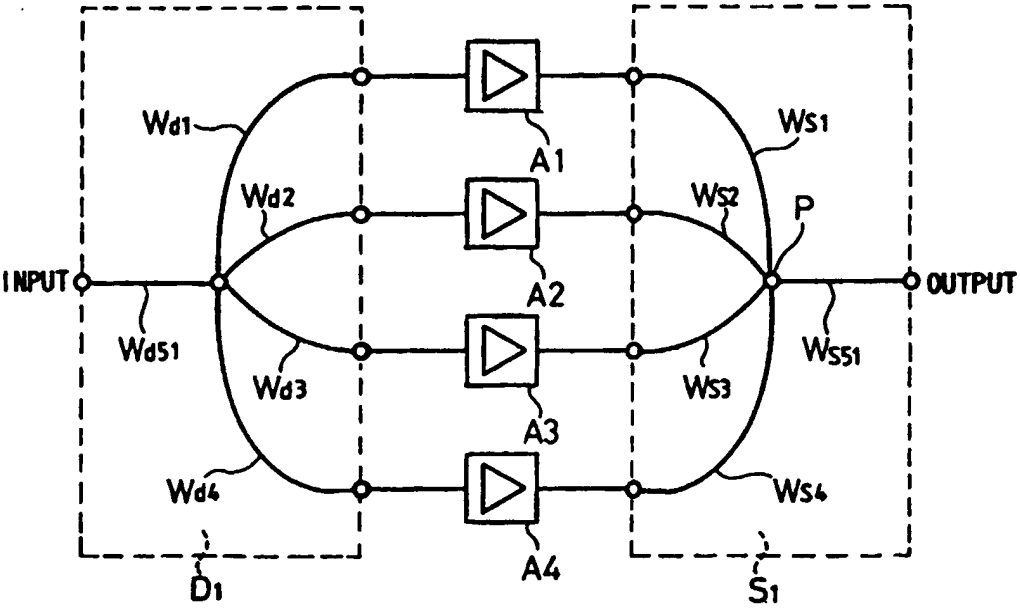

Wd1
Ws1
A1
Wd2
Ws2
P
INPUT
OUTPUT
A2
Wd51
Ws51
Wd3
Ws3
A3
Wd4
Ws4
A4
D1
S1

FIG.3

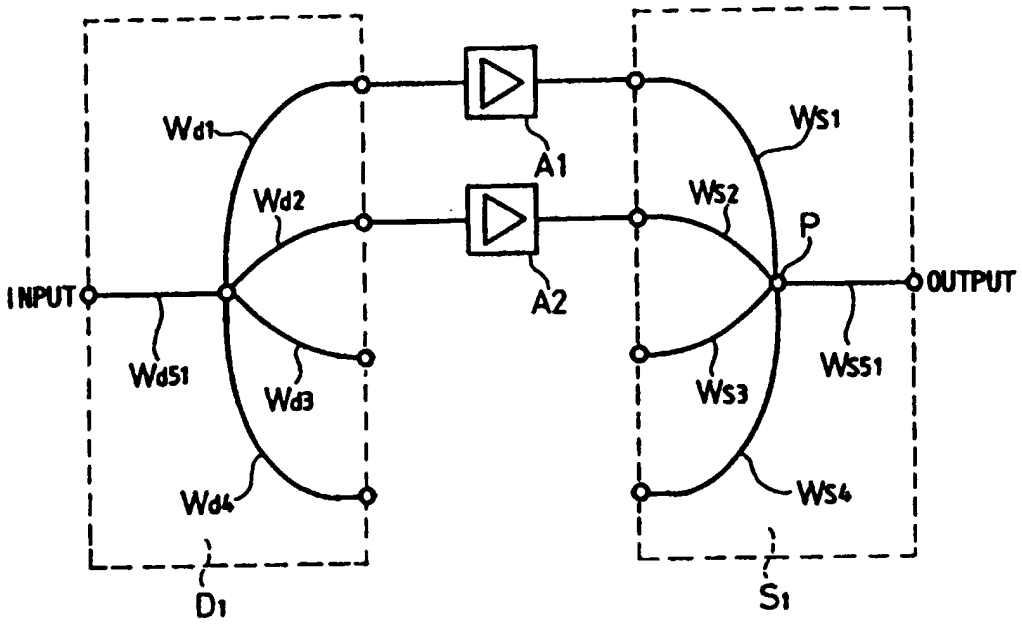

Wd1
Wd2
INPUT
Wd51
Wd3
Wd4
D1
A1
A2
Ws1
Ws2
P
OUTPUT
Ws51
Ws3
Ws4
S1

FIG.4

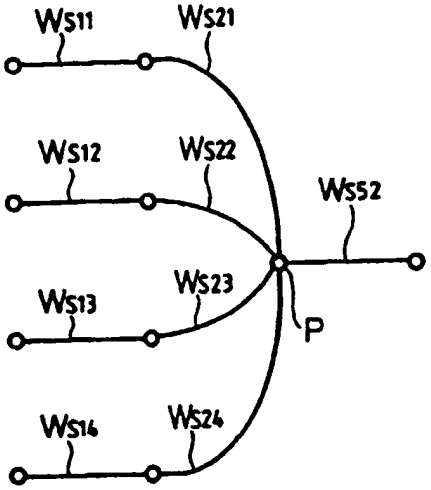

WS11
WS21
WS12
WS22
WS52
WS23
WS13
P
WS14
WS24

FIG.5

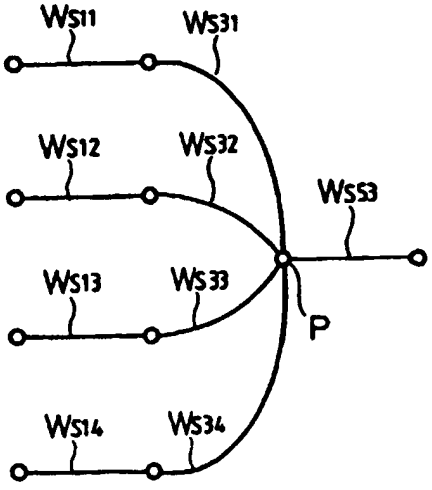

WS11
WS31
WS12
WS32
WS53
WS13
WS33
P
WS14
WS34

FIG.6(A)

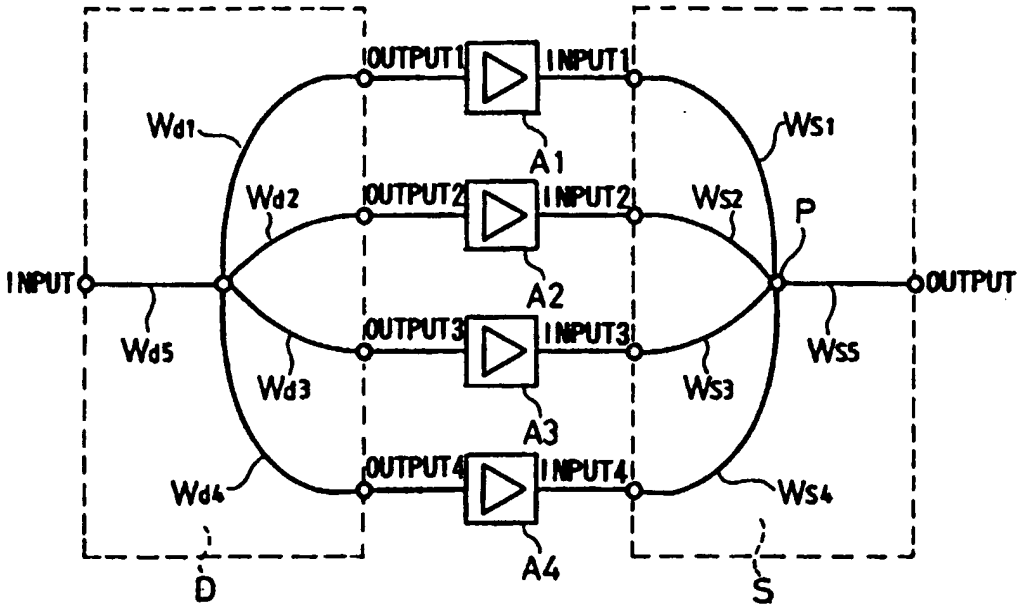

OUTPUT1
INPUT1
A1
Wd1
Ws1
Wd2
OUTPUT2
INPUT2
Ws2
P
A2
INPUT
OUTPUT
Wd5
OUTPUT3
INPUT3
Ws5
Wd3
Ws3
A3
OUTPUT4
INPUT4
Wd4
Ws4
A4
D
S

FIG.6(B)

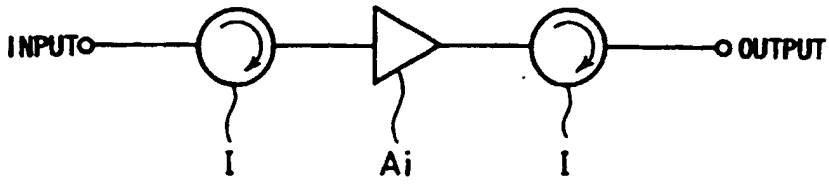

INPUT
OUTPUT
I
Ai
I

FIG.7

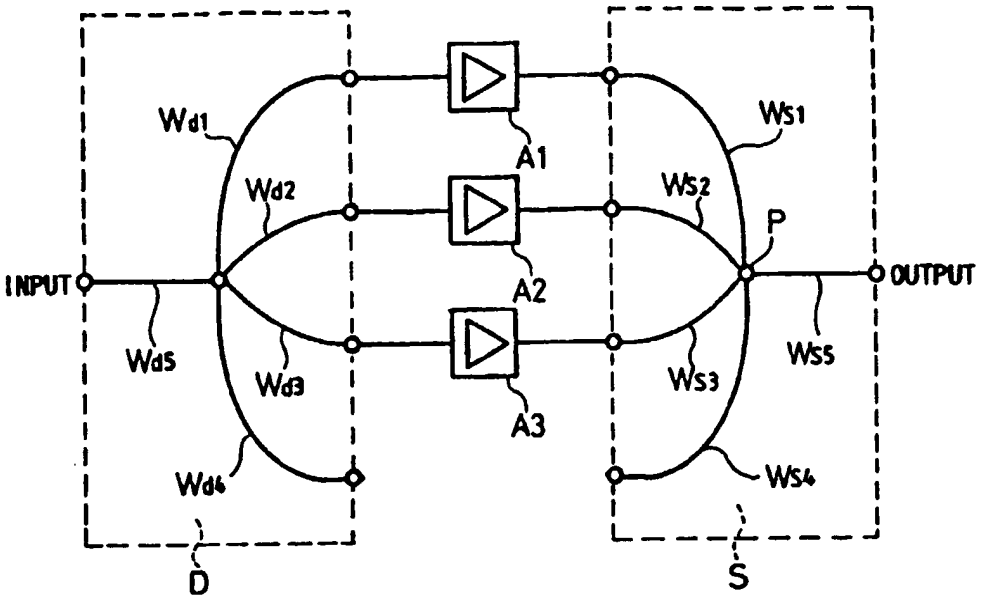
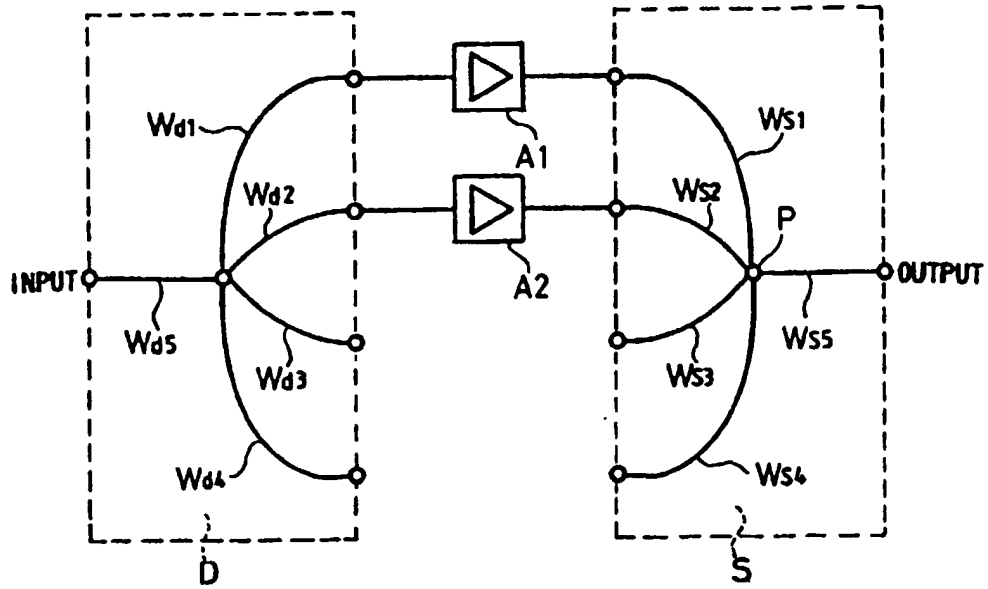

Wd1
Wd2
Wd5
Wd3
Wd4
A1
A2
A3
Ws1
Ws2
P
Ws5
Ws3
Ws4
INPUT
OUTPUT
D
S

FIG.8


Wd1
Wd2
Wd5
Wd3
Wd4
A1
A2
Ws1
Ws2
P
Ws5
Ws3
Ws4
INPUT
OUTPUT
D
S